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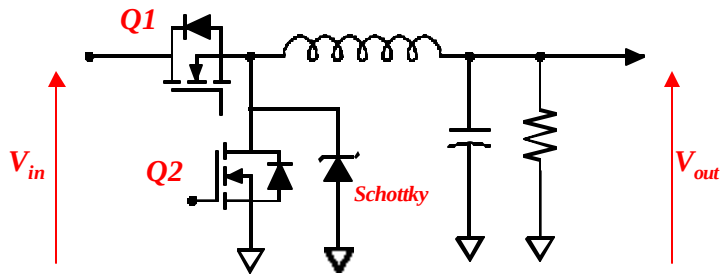
Dual FETKY Integrates All Power Devices for a Synchronous Buck, Enabling Up to 96 Percent Efficiency

Increased demands are being placed upon the system designers of portable equipment for ever reducing form factors, making the trend for increased integration for sub-systems more critical. From system level down to component level, it is important to reduce the size or space taken up by any given solution to enable the user's demanding requirement of smaller, more portable equipment. The designer desires reduction in solution footprint without any significant trade off in efficiency. This is because any trade off in efficiency due to electrical performance will degrade the performance and reliability of the system and have an adverse effect on thermal management.

One example of a portable system with high demands for reduced form factor and high requirements for improved efficiency is the notebook PC. The trends show that notebook PC's are reducing in size at an alarming rate, and with each reduction, they need to squeeze the power for next generation microprocessors. In order to satisfy this market trend, power semiconductor manufacturers are focused on maximizing efficiency in reduced footprints, achieving new higher levels of power density.

Notebook PCs, as well as many other portable systems, use several one-stage Synchronous Buck DC-DC converters that convert a high input voltage down to a low output voltage. In a notebook PC there is one input voltage that can vary between 7.5 V up to 21 V, depending on whether it is fed by its battery or operating from an AC adapter, and there are several output voltages: 1.3 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V. Each output voltage has its own circuit that needs special consideration, as shown in Figure 1, in order to optimize performance. The 1.8 V, 3.3 V and 5.0 V all have approximately the same maximum output currents, at 4-5 Apk under worst case conditions, and are typically used for supplying peripheral appliances or devices within the notebook PC.

Figure 1. Synchronous Buck DC-DC converter topology used for 1.8V, 3.3V & 5.0V peripheral applications in notebook PCs.

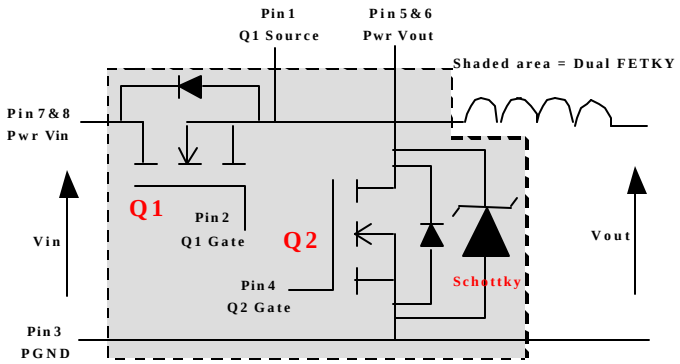


Enabling reduced form factors by increasing power density.

Advances have been made in silicon technologies in recent years, mainly being driven by core CPU applications, requiring up to 15 Apk at a lower output voltage of 1.3 V. These silicon technologies harness the qualities that are required for optimum performance in other DC-DC applications. The high side, control FET (Q1) requires low combined Q_{sw}[1] and $R_{DS}(on)$, where Q_{sw} is the portion of gate charge that causes a power loss during the switching phase of operation, and $R_{DS}(on)$ is the on-state resistance of the FET that causes a power dissipation during conduction. The low side, synchronous FET (Q2) requires low $R_{DS}(on)$ and high Cdv/dt immunity, where $R_{DS}(on)$ is the on-state resistance of the FET that causes a power loss during conduction, and Cdv/dt is a phenomena that needs some explanation. Cdv/dt is a parameter used to understand an "unintended turn-on" of Q2. This can occur if the rise of voltage on the drain of Q2 is fast enough to cause a voltage spike on the gate of Q2 through a capacitive coupling. If this spike on the gate of Q2 exceeds the threshold voltage, Q2 will turn on, causing a short circuit condition to occur because Q1 will also be turned on at this point in the switching sequence. To obtain Cdv/dt "immunity," a charge ratio on Q2 needs to be optimized. This ratio is defined as $Q_{GD}/Q_{GS1} \leq 1$, where Q_{GD} is gate-to-drain charge, and Q_{GS1} is pre-threshold gate-to-source charge.

By using next generation silicon platforms, a solution can be developed for lower power DC-DC converters. An example of such a product is the Dual FETKY™ from International Rectifier. The Dual FETKY, or IRF7901D1, is an integrated solution for DC-DC converters. It includes all the power semiconductor devices for synchronous buck applications, integrating a 30 V n-channel high side control FET (Q1), a 30 V n-channel low side synchronous FET (Q2) and a 30 V parallel schottky diode for Q2. The Dual FETKY also moves toward the "componentizing" of the DC-DC converter. The Dual FETKY includes interconnects that minimize external PCB traces that would be necessary if discrete components were used, as shown in Fig.2. Internal interconnects also provide a lower inductance path, critical for high frequency switching applications.

Figure 2. IRF7901D1 Dual FETKY™, co-packages two MOSFETs and a schottky diode.



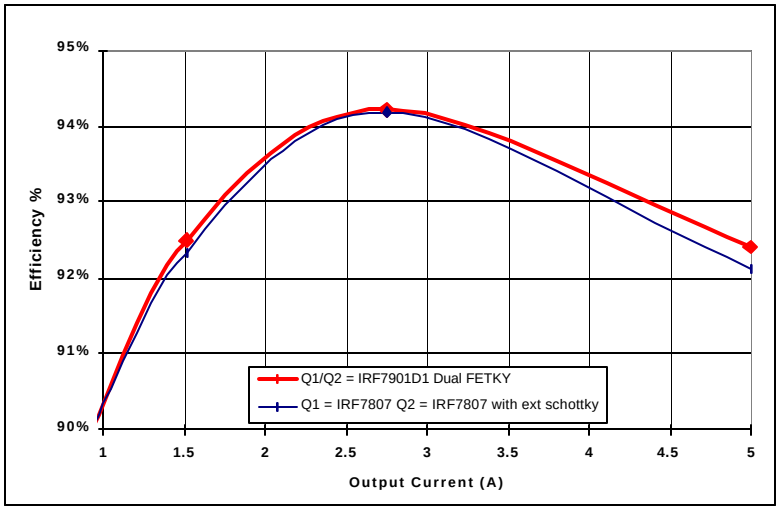
Pin nomenclature has been changed to represent a functional block in order to make it easier to interface with the rest of the system. Conventional discrete component terminology is removed to be replaced with more conventional power conversion terminology, like PGND, Pwr Vin, Pwr Vout, etc. The Dual FETKY specification is shown in Table 1.

Table 1. Short form specification of the Dual FETKY IRF7901D1.

	IRF7901D1 – Dual FETKY™		
Parameter	**Control FET Q1**	**Synchronous FET Q2**	**Schottky**
V_{DS}	30V	30V	-
V_{GS}	+/- 20V	+/- 20V	-
$R_{DS}(on)$	28.5mΩ	22mΩ	-
$Q_G(typ)$	7.6nC	13.6nC	-
$Q_{switch}(typ)$	2.4nC	5.7nC	-
$V_F(typ)$	-	-	0.48V
$R_{\theta JA}(max)$	62.5°C/W		
$R_{\theta JL}(max)$[2]	25°C/W		

Table 1 shows the key device parameters for the Dual FETKY. Silicon technologies were selected to get the most optimized die for the application, thus resulting with a Q1 with 28.5 mΩ on-state resistance and 2.4 nC of switching charge and Q2 with 22 mΩ on-state resistance. Also Q2 has a charge ratio of 0.87, providing immunity to unintended turn on.

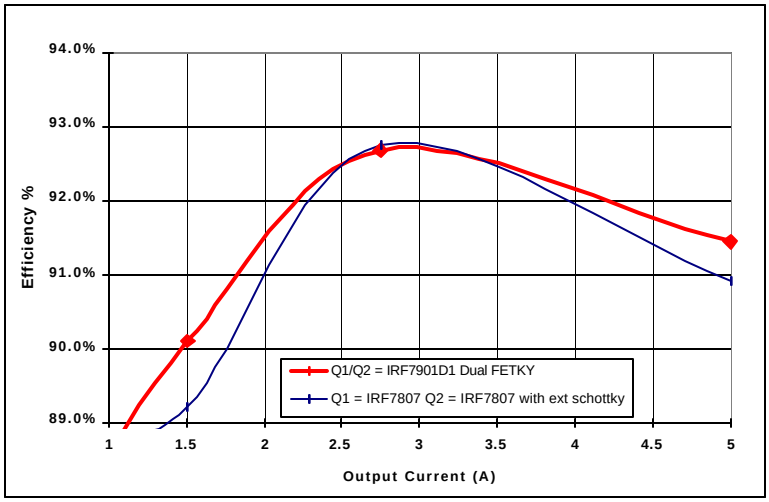
Figure 3a. Electrical efficiency curves for 14Vin / 3.3Vout / 300kHz



Fully integrated Dual FETKY solution achieves up to 60% space saving

The IRF7901D1 obtains up to 96 percent and 94 percent typical efficiency in 5.0 Vout and 3.3 Vout applications, respectively. The overall efficiency is shown in Fig 3a, b, c, d across the whole range of load currents for peripheral DC-DC applications in notebook PCs.

Figure 3b. Electrical efficiency curves for 21Vin / 3.3Vout / 300kHz



Space saving Dual FETKY achieves ~0.5% eff advantage at max & light loads

Figure 3c. Electrical efficiency curves for 14Vin / 5.0Vout / 300kHz

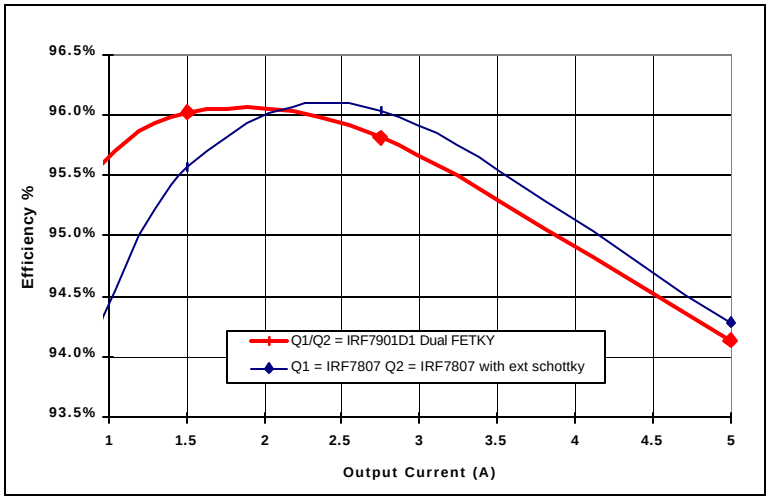
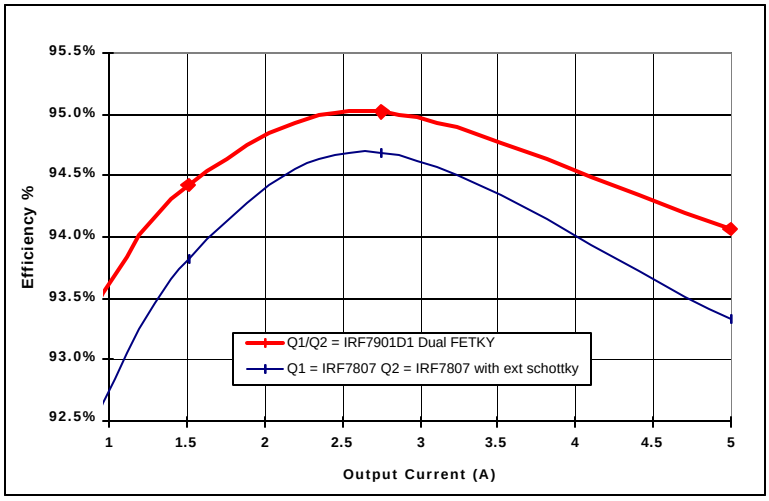


Figure 3d. Electrical efficiency curves for 21Vin / 5.0V / 300kHz



For 5.0V applications, up to 1% advantage across all load conditions can be obtained

Figure 3a and 3b show the performance for 3.3 V_{out} applications, and Figure 3c and 3d show the performance for 5.0 V_{out} applications for Dual FETKY versus IR's discrete alternate solution. The IR discrete solution is a three-device solution, using two SO-8 packages plus an external schottky. The Dual FETKY achieves this level of performance by co-packaging two FETs and the schottky in a single SO-8 package. This gives up to 60 percent board space saving and, on aggregate across the operating conditions shown, gives better performance.

Thermal performance is also very important. It is undesirable for the semiconductors to get too hot, since this will degrade their reliability and also cause adverse effects to the system temperature. Typically, 26 watts of power dissipation within a notebook PC will give the maximum allowable skin temperature for the system. Every little improvement in electrical and thermal efficiency helps to enable this goal. Figure 4 shows the thermal performance of the Dual FETKY at worst case conditions for both the 3.3V_{out} and 5.0V_{out} applications[3].

The thermal images in Figure 4, show PCB temperatures and maximum case temperatures. It is estimated that the junction will be no hotter than 3°C above the maximum case temperature[4]. A summary of the results can be seen in Table 3.

Figure 4. Thermal Efficiency images for Dual FETKY.

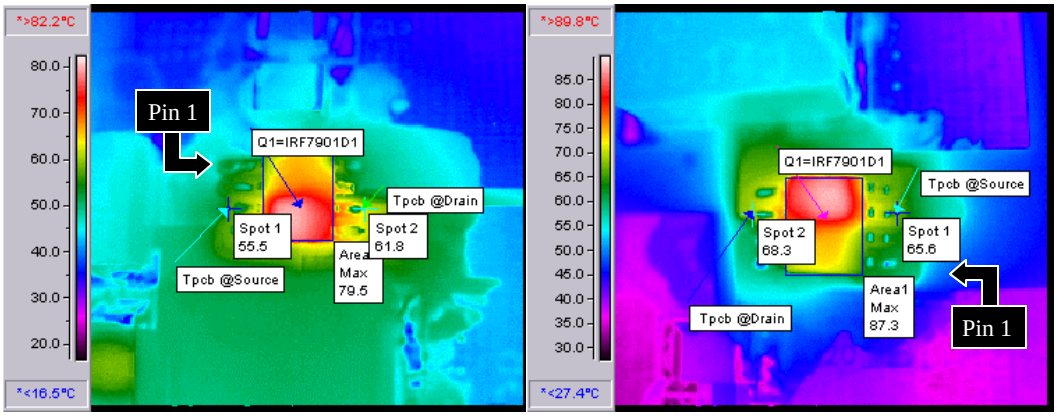


Fig 4a. 21V_{in} / 3.3V_{out} / 5A_{cont} **Fig 4b. 21V_{in} / 5.0V_{out} / 5A_{cont}**

Table 3. Summary of IRF7901D1 Dual FETKY thermal performance images.

Operating Conditions			Temperatures (°C)				
V_{in}	V_{out}	I_{out} continuous[3]	T_{case}	T_J	T_{PCB}	DT_{J-PCB}	$T_{J\,max}$ if T_{PCB}=90° C
21V	3.3V	5A	79.5°C	82.5°C	58.7°C	23.8°C	115.0°C
21V	5.0V	5A	87.3°C	90.3°C	67.0°C	23.3°C	115.0°C

The data shows that if the IRF7901D1 Dual FETKY is operated at maximum conditions, there is significant safety margin before exceeding the maximum rated temperature of the silicon, which is 150°C. Also included is an estimate of the maximum junction temperature if the PCB board temperature reaches 90°C. This is considered to be a maximum allowable temperature for the PCB inside a notebook PC. Even if this condition occurs, the maximum junction temperature will be 115°C, including increased on-state resistance due to the temperature coefficient.

[1] Refer to IRF7805 / IRF7807 datasheet for a more detailed explanation
[2] Junction-to-Lead thermal resistance measured on design kit IRNBPS2. Measured as device junction temperature (T_J) to power leads (V_{in} & V_{out}).
[3] Test conditions were maintained for 5 minutes.
[4] Refer to International Rectifier Design Tip DT 99-2.